PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Kenneth Rose; Mick Jacobs; Jatin Batra		
Assignee:	Cisco Technology, Inc.		
Title:	ADAPTIVE BANDWIDTH UTILIZATION OVER FABRIC LINKS		
Application No.:	09/978,475	Filing Date:	October 16, 2001
Examiner:	Karen C. Tang	Group Art Unit:	2447
Docket No.:	CIS0128US	Confirmation No.:	5139

Austin, Texas
October 3, 2011

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APPEAL BRIEF

Dear Sir:

This brief is submitted in support of the Notice of Appeal filed on May 27, 2011 by the Appellants to the Board of Patent Appeals and Interferences from the Examiner's rejection of claims in the Final Office Action of January 31, 2011. The appellant notes that the appeal filed was received at the Office on May 27, 2011. This brief follows the Notice of Panel Decision that was mailed on July 1, 2011 , which specified a one-month period for submission of this brief.

Filed herewith is a Petition for Extension of Time requesting a two-month extension, thereby giving the undersigned a period until October 3, 2011 in which to respond since October 1, 2011 falls on a Saturday. Please charge deposit account No. 502306 for the fee associated with this Appeal Brief. Please charge this deposit account for any additional sums which may be required to be paid as part of this appeal.

REAL PARTY IN INTEREST

The real party in interest on this appeal is the assignee, CISCO TECHNOLOGY, INC., as named in the caption above.

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to this application.

STATUS OF CLAIMS

Claims 1-4, 6-8, 10-12, 14-16, 24-27, 30-32, 34, and 35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,990,073 issued to Sandoval ("Sandoval") in view of U.S. Patent No. 6,907,001 issued to Nakayama et al. ("Nakayama"), and further in view of Bass, U.S. Patent Publication No. 2003/0035373 ("Bass"). Claims 5, 7, 9, 13, 15, 17-23, 26-29, 33, and 36-43 are cancelled or presumed cancelled.

STATUS OF AMENDMENTS

Concurrently filed with this paper is an amendment cancelling claims 37-43.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a method that includes receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time. *See, e.g.,* Page 8, lines 16-17, and Figure 2B. A first data quantity value representing a quantity of data stored in the memory is generated at a first point in time. *See, e.g.,* Page 8, lines 22-28, and Figure 2B. The first data quantity value is compared to a first predetermined value. *See, e.g.,* Page 9, lines 22-24, and Figure 2B. The transmitting device transmits data at a second non-zero rate to the

memory for storage therein during a second period of time in response to the comparing. *See, e.g.,* Page 15, lines 21-23, and Figure 2A. The first predetermined value is modified in response at least in part to the comparing the first data quantity value to the first predetermined value. *See, e.g.,* Page 16, lines 18-26. The second period of time is subsequent to the first period of time. *See, e.g.,* Page 15, lines 21-23, Figure 2A, and Figure 4. The second non-zero rate is greater than the first non-zero rate. *See, e.g.,* Page 15, lines 6-13, and Figure 5.

Independent claim 10 recites an apparatus comprising a memory device configured to receive data from a transmitting device for storage therein. *See, e.g.,* Page 8, lines 16-17, and Figure 2B. A first circuit is configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate. *See, e.g.,* Page 9, lines 11-14, and Figure 2B. A second circuit is configured for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time. *See, e.g.,* Page 8, lines 22-28, and Figure 2B. A first comparing circuit is configured for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing. *See, e.g.,* Page 9, lines 22-24, Page 10, lines 11-12, and Figure 2B. A circuit is configured for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value. *See, e.g.,* Page 16, lines 18-26.

Independent claim 24 recites an apparatus comprising a memory device configured to receive data from a transmitting device for storage therein. *See, e.g.,* Page 8, lines 16-17, and Figure 2B. A first means is configured for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate. *See, e.g.,* Page 9, lines 11-14, and Figure 2B. A second means is configured for generating a first data quantity value representing a quantity of data stored

in the memory device at a first point in time. *See, e.g.,* Page 8, lines 22-28, and Figure 2B. A third means is configured for comparing the first data quantity value to a first predetermined value. *See, e.g.,* Page 9, lines 22-24, Page 10, lines 11-12, and Figure 2B. A means is configured for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value. *See, e.g.,* Page 16, lines 18-26. The first means is configured to generate the rate control signal in response to the comparing. *See, e.g.,* Page 9, lines 22-24, Page 10, lines 11-12, and Figure 2B.

Dependent claim 27 recites a fourth means for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time. *See, e.g.,* Page 8, lines 23-29, and Figure 3. A fifth means is configured for comparing the first data quantity value to the second data quantity value. *See, e.g.,* Page 14, lines 2-6, and Figures 3 and 4. The first means is further configured to generate the rate control signal only if the first data quantity value is not equal to the second data quantity value. *See, e.g.,* Page 14, lines 6-7, and Figures 3 and 4.

Independent claim 30 recites a method comprising receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time. *See, e.g.,* Page 8, lines 16-17, and Figure 2B. A rate control signal is generated by generating a first data quantity value representing a quantity of data stored in the memory at a first point in time. *See, e.g.,* Page 14, lines 13-22, and Figures 3 and 4. The first data quantity value is compared to a first predetermined value, wherein the rate control signal is generated in response to the comparing. *See, e.g.,* Page 14, lines 13-22, and Figures 3 and 4. The transmitting device is caused to transmit data at a second non-zero rate to the memory for storage therein during a second period of time, wherein the causing comprises transmitting the rate control signal to the transmitting device. *See, e.g.,* Page 9, lines 11-14, and Figure 2B. The first predetermined value is modified in response at least in part to the comparing the first data quantity value to the first predetermined value. *See, e.g.,* Page 16, lines 18-26. The second period of time is subsequent to the first period of time. *See, e.g.,* Page 15,

lines 21-23, Figure 2A, and Figure 4. The second non-zero rate is less than the first non-zero rate. *See, e.g.,* Page 15, lines 6-13, and Figure 5.

Independent claim recites 31an apparatus comprising a memory device configured to receive data from a transmitting device for storage therein. *See, e.g.,* Page 8, lines 16-17, and Figure 2B. A first circuit is configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate, wherein the second non-zero rate is less than the first non-zero rate. *See, e.g.,* Page 9, lines 11-14, and Figure 2B. A second circuit is configured for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time. *See, e.g.,* Page 8, lines 22-28, and Figure 2B. A first comparing circuit is configured for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing. *See, e.g.,* Page 9, lines 22-24, Page 10, lines 11-12, and Figure 2B. A circuit is configured for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value. *See, e.g.,* Page 16, lines 18-26.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection of independent claims 1, 10, 24, 30, and 31.

The rejection of dependent claims 7, 15, and 27.

The rejection of dependent claim 14.

ARGUMENT

All pending claims stand rejected under 35 U.S.C. § 103 as being unpatentable over Sandovol in view of Nakayama and in further view of Bass. In order for a claim to be rendered invalid under 35 U.S.C. §103, the subject matter of the claim as a whole would have to be obvious to a person of ordinary skill in the art at the time the invention was made. *See* 35 U.S.C. §103(a). This requires: (1) the reference(s) must teach or suggest all of the claim limitations; (2) there must be some teaching, suggestion or motivation to combine references either in the references themselves or in the knowledge of the art; and (3) there must be a reasonable expectation of success. *See* MPEP 2143; MPEP 2143.03; *In re Rouffet*, 149 F.3d 1350, 1355-56 (Fed. Cir. 1998).

I. The rejection of independent claims 1, 10, 24, 30, and 31

Independent claim 1 has been substantially narrowed since it was first filed. Originally filed claim 1 was directed to a method for adjusting the rate at which data was transmitted to memory for storage therein. During prosecution, the claim was amended to include an act of comparing the quantity of data in the memory with a predetermined value, and adjusting the data transmission rate based on the comparison. Claim 1 was then further limited to its current state, which now recites an act of modifying the predetermined value is in response to the comparison. Specifically, independent claim 1 recites, "modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value." The Final Office Action admits that neither that Sandoval nor Nakayama disclose the claimed "modifying" limitation. The FOA on page 4 argues, however, that Bass teaches this missing limitation in paragraph 0019. Appellants respectfully disagree.

Bass describes use of thresholds of information in queues to prevent underflow and overflow of the queues. *See* Bass, paragraph 0002. With reference to Figure 1 of Bass, a rate controller 108 sets the transmit rate of a transmitter 104 at transmit rates Tr=0, Tr=Max/2 and Tr=Max where Max denotes the maximum transmit rate of the transmitter. The controller is responsive to an updated transmit rate received from a destination 112 via a signal receiving unit 114. *See* Bass, paragraph 0018.

Bass describes, "The threshold circuit 130 calculates and sets a lower threshold T1 and an upper threshold T2 in the buffer 124 based upon Max value 132, Qmax value 134." The thresholds T1 and T2 are the thresholds in the buffer 124 used to prevent underflow and overflow, respectively. A destination 112 receives data packets that are subsequently provided to buffer queue 124 having a maximum capacity of Qmax. The threshold circuit 130 periodically provides an updated transmit rate. *See* Bass, paragraph 0019

In one embodiment, if the data packet level stored in the buffer is greater than T2, then an updated transmit rate of 0 is communicated to the sender. Else, if the level of data packets stored in the buffer is greater than T1, then a transmit rate of Max/2 is communicated to the sender. Else, a transmit rate of Max is communicated to the sender. *See* Bass, paragraph 0020

Claim 1 requires modification of the first predetermined value. The FOA equates T1 and/or T2 of Bass with the claimed first predetermined value. However, neither T1 nor T2 is modified in paragraph 0019 of Bass as alleged in the FOA. Further, Appellants cannot identify any other section of Bass, which teaches modification of T1 or T2, let alone modification of T1 or T2 after they are compared with the quantity of data in buffer

124. Rather, paragraph 0063 of Bass indicates that T1 and T2 are computed "at initialization time from Qmax." At the very least, nothing within paragraph 0019 of Bass indicates that T1 or T2 is modified. Thus, paragraph 0019 of Bass does not teach "modifying the first predetermined value."

In addition to Bass failing to teach modifying T1 or T2, Bass fails to teach the temporal relationship required between the comparing and modifying steps. Claim 1 requires "modifying the first predetermined value is made in response to comparing the first data quantity value to the first predetermined value." Bass teaches a circuit 134 calculates T1 and T2 at initialization, and a threshold circuit that compares T1 and T2 to the level of data packets temporarily stored in buffer queue 124. *See* Bass, paragraphs 0063 (emphasis added) and 0019. This section of Bass indicates that T1 and T2 are calculated before any comparison is made with data stored in queue 124. Thus, the rejection of claim 1 is in error.

Independent claim 10 recites a limitation similar to the limitation of claim 1 argued above. Specifically, independent claim 10 recites "a circuit for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value." The FOA rejects independent claim 10 using the same rationale that was used to reject claim 1. See FOA, pages 6 and 7. Appellants submit this rejection is in error for the same or similar reasons argued above that the rejection of claim 1 is in error.

Independent claim 24 recites a limitation similar to the limitation of claim 1 argued above. Specifically, independent claim 10 recites "a means for modifying the first predetermined value in response at least in part to the comparing the first data quantity

submit this rejection is in error for the same or similar reasons argued above that the rejection of claim 1 is in error.

Independent claim 30 recites a limitation similar to the limitation of claim 1 argued above. Specifically, independent claim 10 recites "modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value." The FOA rejects independent claim 10 using the same rationale that was used to reject claim 1. See FOA, pages 11 and 12. Appellants submit this rejection is in error for the same or similar reasons argued above that the rejection of claim 1 is in error.

Independent claim 31 recites a limitation similar to the limitation of claim 1 argued above. Specifically, independent claim 10 recites "modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value." The FOA rejects independent claim 10 using the same rationale that was used to reject claim 1. See FOA, pages 12 and 13. Appellants submit this rejection is in error for the same or similar reasons argued above that the rejection of claim 1 is in error.

II. The rejection of dependent claims 7, 15, and 27

Dependent claim 7 includes all the limitations of dependent claim 4 and independent claim 1. Dependent claim 7 recites comparing data quantities stored in the memory device at different times. The FOA argues that Bass, paragraphs 0019 and 0020 teach these limitations. Appellants respectfully disagree. In arguments above, Appellants point out that paragraphs 0019 and 0020 of Bass teach comparing quantity of data in buffer 124 with T1 or T2, not with the quantity of data in buffer 124 at another time as required by claim 7. Accordingly, the rejection of claim 7 is in error.

Dependent claim 15 includes all the limitations of independent claim 10. Dependent claim 15 recites a second circuit for comparing data quantities stored in the memory device at different times. The FOA argues that Bass, paragraphs 0019 and 0020 teach these limitations. Appellants respectfully disagree. In arguments above, Appellants point out that paragraphs 0019 and 0020 of Bass teach comparing quantity of data in buffer 124 with T1 or T2, not with the quantity of data in buffer 124 at another time as required by claim 15. Accordingly, the rejection of claim 15 is in error.

Dependent claim 27 includes all the limitations of independent claim 24. Dependent claim 27 recites a fifth means for comparing data quantities stored in the memory device at different times. The FOA argues that Bass, paragraphs 0019 and 0020 teach these limitations. Appellants respectfully disagree. In arguments above, Appellants point out that paragraphs 0019 and 0020 of Bass teach comparing quantity of data in buffer 124 with T1 or T2, not with the quantity of data in buffer 124 at another time as required by claim 27. Accordingly, the rejection of claim 27 is in error.

III. The rejection of dependent claim 14

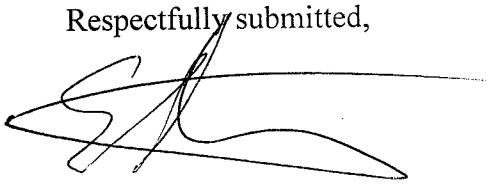
Dependent claim 14 includes all the limitations of independent claim 10 in addition to a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values. The FOA on page 8 argues that Sandoval in column 3, line 35 - column 4, line 15 teaches a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values. Appellants respectfully disagree. Column 3, line 35 - column 4, line 15 of Sandoval teaches a single test circuit 120. This test circuit 120 uses an average queue depth to detect symptoms of congestion in FIFO buffer 126. If the average queue depth is below the minimum

threshold, then test circuit 120 permits an additional data packet to enter FIFO 126 for storage. The FOA equates the Sandoval's test circuit 120 with the claimed first comparing circuit. See FOA, pages 6 and 7. Column 3, line 35 - column 4, line 15 does not teach multiple test circuits 120. Accordingly, Column 3, line 35 - column 4, line 15 cannot teach the required multiple comparing circuits. Accordingly, Appellants submit that the rejection of dependent claim 14 is in error.

CONCLUSION

For the above reasons, Appellant respectfully submits that the rejection of pending Claims 1-4, 6, 8, 10-12, 14, 16, 24, 25, 30-32, 34, 35 and 37-43 is unfounded. Accordingly, Appellant respectfully requests that the Board reverse the rejections of these claims.

Respectfully submitted,



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CLAIM APPENDIX

1. (Previously Presented) A method comprising:

receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time;

generating a first data quantity value representing a quantity of data stored in the memory at a first point in time,

comparing the first data quantity value to a first predetermined value;

causing the transmitting device to transmit data at a second non-zero rate to the memory for storage therein during a second period of time, in response to the comparing;

modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the second period of time is subsequent to the first period of time; and wherein the second non-zero rate is greater than the first non-zero rate.

2. (Previously Presented) The method of claim 1 wherein the memory device comprises a FIFO buffer.

3. (Original) The method of claim 1 wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

4. (Previously Presented) The method of claim 1 further comprising:

generating a rate control signal; and

transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate;

wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

5. (Cancelled)

6. (Previously Presented) The method of claim 4 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

7. (Previously Presented) The method of claim 4 further comprising:

generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

comparing the first data quantity value to the second data quantity value;

wherein the rate control signal is generated only if the first data quantity value is not equal to the second data quantity value.

8. (Previously Presented) The method of claim 1 wherein generating the first data quantity value comprises:

generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time;

generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period of time ending in the first point in time;

subtracting the total data output count from total data input count.

9. (Cancelled)

10. (Previously Presented) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate;

a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time;

a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing; and

a circuit for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value.

11. (Original) The apparatus of claim 10 wherein the memory device comprises a FIFO buffer.

12. (Original) The apparatus of claim 10 further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

13. (Cancelled)

14. (Previously Presented) The apparatus of claim 10 further comprising:

a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values, wherein the first comparing circuit is one of the plurality of comparing circuits, and wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the first circuit generates the rate control signal in response to comparing the first data quantity value to the plurality of predetermined values.

15. (Previously Presented) The apparatus of claim 10 further comprising:

a third circuit for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

a second comparing circuit for comparing the first data quantity value to the second data quantity value;

wherein the first circuit generates the rate control signal only if the first data quantity value is not equal to the second data quantity value.

16. (Original) The apparatus of claim 15 wherein the first and second circuits are the same circuits.

17. – 23 (Cancelled)

24. (Previously Presented) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first means for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate;

a second means for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time; a third means for comparing the first data quantity value to a first predetermined value; and

a means for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the first means generates the rate control signal in response to the comparing.

25. (Original) The apparatus of claim 24 wherein the memory device comprises a FIFO buffer.

26. (Original) The apparatus of claim 24 further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

27. (Previously Presented) The apparatus of claim 24 further comprising:

a fourth means for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

a fifth means for comparing the first data quantity value to the second data quantity value;

wherein the first means generates the rate control signal only if the first data quantity value is not equal to the second data quantity value.

28. (Cancelled)

29. (Cancelled)

30. (Previously Presented) A method comprising:

receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time;

generating a rate control signal by

generating a first data quantity value representing a quantity of data stored in the memory at a first point in time,

comparing the first data quantity value to a first predetermined value, wherein

the rate control signal is generated in response to the comparing;

causing the transmitting device to transmit data at a second non-zero rate to the memory for storage therein during a second period of time, wherein

the causing comprises transmitting the rate control signal to the transmitting device; and

modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the second period of time is subsequent to the first period of time; and

wherein the second non-zero rate is less than the first non-zero rate.

31. (Previously Presented) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate, wherein the second non-zero rate is less than the first non-zero rate;

a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time;

a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing; and

a circuit for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value.

32. (Previously Presented) The method of claim 30 further comprising:

transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate; and

wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

33. (Cancelled)

34. (Previously Presented) The method of claim 32 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

35. (Previously Presented) The method of claim 1 wherein the causing comprises:

transmitting a rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate, wherein

the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

36. (Cancelled)

37. (Previously Presented) The method of claim 35 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

38. (Previously Presented) The method of claim 1 further comprising

the transmitting device transmitting data at a third non-zero rate to the memory for storage therein during a third period of time;

wherein the third period of time is subsequent to the second period of time, and wherein the third non-zero rate is greater than the second non-zero rate.

39. (Previously Presented) The method of claim 44, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

40. (Previously Presented) The apparatus of claim 45, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

41. (Previously Presented) The apparatus of claim 46, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

42. (Previously Presented) The apparatus of claim 47, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

43. (Previously Presented) The apparatus of claim 48, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

44-48. (Cancelled)

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None